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09/253,995	02/22/1999	YOSHIHIRO SAGA	B208-1021	6335

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EXAMINER
HANNETT, JAMES M

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/253,995	Applicant(s) SAGA, YOSHIHIRO
	Examiner James M Hannett	Art Unit 2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/22/1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-40 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,146,592 Pfeiffer et al.

As for Claim 1, Pfeiffer et al teaches in the abstract the use of an image processing apparatus. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor.

As for Claim 2, Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor.

In regards to Claim 3, Pfeiffer et al teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

In regards to Claim 4, Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

As for Claim 5, Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

In regards to Claim 6, Pfeiffer et al teaches on Columns 9, Lines 7-22 that the image algorithm processor controls the requests for memory access of the image memory. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks. Pfeiffer et al teaches that the image algorithm processor controls the access requests from all of the image processors and teaches that the parallel

processor set can perform more than one process. Therefore, enabling the image processing apparatus with control means to control another operation of the image processing apparatus. Pfeiffer et al teaches on Columns 20, Lines 27-46 that a portion of the image memory is not viewable and allows image processing data, such as coefficients, intermediate results or instructions to be stored in the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor Pfeiffer et al teaches that no two address requests can request access to the image memory simultaneously. Therefore, the access request to store image processing instructions to the image memory will be carried out at a time other than a time during which a refresh process, first process, or second process access the image memory.

As for Claim 7, Pfeiffer et al teaches on Column 22, Lines 33-40 and depicts in Figure 8 the use of a DRAM refresh controller that includes a refresh interval timer (242) that increments a count value by one within the predetermined refresh timing period required. Pfeiffer et al teaches that performing the refresh operation will decrement or decrease the (DRRFREQ) signal to zero. Pfeiffer et al further teaches that the refresh operation is only performed when the value of (DRRFREQ) is not equal to zero.

As for Claim 8, Claim 8 is rejected for reasons discussed related to Claim 1, since Claim 1 is substantively equivalent to Claim 8.

As for Claim 9, Claim 9 is rejected for reasons discussed related to Claim 2, since Claim 2 is substantively equivalent to Claim 9.

As for Claim 10, Pfeiffer et al teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

As for Claim 11, Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

As for Claim 12, Claim 12 is rejected for reasons discussed related to Claim 5, since Claim 5 is substantively equivalent to Claim 12.

In regards to Claim 13, Claim 13 is rejected for reasons discussed related to Claim 1, since Claim 13 is substantively equivalent to Claim 1.

As for Claim 14, Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor. The refresh operation is synchronized with the output image data in that the refresh period is performed during the horizontal blanking period of the image data being displayed on the monitor.

As for Claim 15, Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially

loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor. Therefore, the refresh cycle is synchronized with the horizontal synchronizing signal.

In regards to Claim 16, Pfeiffer et al teaches on Column 22, Lines 55-62 a time period constituting the amount of time needed between each DRAM refresh sequence for the type of DRAM chip can be programmed into memory. Pfeiffer et al teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

In regards to Claim 17, Pfeiffer et al teaches on Columns 9, Lines 7-22 that the image algorithm processor controls the requests for memory access of the image memory. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks. Pfeiffer et al teaches that the image algorithm processor controls the access requests from all of the image processors and teaches that the parallel processor set can perform more than one process. Therefore, enabling the image processing apparatus with control means to control another operation of the image processing apparatus. Pfeiffer et al teaches on Columns 20, Lines 27-46 that a portion of the image memory is not viewable and allows image processing data, such as coefficients, intermediate results or

instructions to be stored in the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor Pfeiffer et al teaches that no two address requests can request access to the image memory simultaneously. Therefore, the access request to store image processing instructions to the image memory will be carried out at a time other than a time during which a refresh process, first process, or second process access the image memory.

As for Claim 18, Pfeiffer et al teaches in the abstract the use of an image processing apparatus. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Columns 9, Lines 7-22 that the image algorithm processor controls the requests for memory access of the image memory. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks. Pfeiffer et al teaches that the image algorithm processor controls the access requests from all of the image processors and teaches that the parallel processor set can perform more than one process. Therefore, enabling the image

processing apparatus with control means to control another operation of the image processing apparatus. Pfeiffer et al teaches on Columns 20, Lines 27-46 that a portion of the image memory is not viewable and allows image processing data, such as coefficients, intermediate results or instructions to be stored in the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor Pfeiffer et al teaches that no two address requests can request access to the image memory simultaneously. Therefore, the access request to store image processing instructions to the image memory will be carried out at a time other than a time during which a refresh process, first process, or second process access the image memory.

As for Claim 19, Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that a refresh request is performed during the horizontal blanking period of the image data being displayed on the monitor.

In regards to Claim 20, Pfeiffer et al teaches in the abstract the use of an image processing apparatus. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of

performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Therefore, in the case of a screen refresh command the DRAM refresh period would follow a screen refresh command. Furthermore, in the case of a request from the image algorithm processor a DRAM refresh period would occur before an image algorithm processor command. Therefore, the period of operation of a DRAM refresh command can be switched depending on whether a screen refresh command or an image algorithm processor command is being executed.

In regards to Claim 21, Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor. Therefore, the refresh cycle is synchronized with the horizontal synchronizing signal.

As for Claim 22, Pfeiffer et al teaches on Column 22, Lines 55-62 a time period constituting the amount of time needed between each DRAM refresh sequence for the type of DRAM chip can be programmed into memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers

is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Therefore, the DRAM refresh process would follow the predetermined refresh timing during an image processing process of the image algorithm. Since the DRAM refresh process processor is given priority over the image algorithm processor.

As for Claim 23, Pfeiffer et al teaches in the abstract the use of an image processing apparatus. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor. Therefore, the refresh cycle is synchronized with the horizontal synchronizing signal.

In regards to Claim 24, Pfeiffer et al teaches on Column 22, Lines 55-62 a time period constituting the amount of time needed between each DRAM refresh sequence for the type of DRAM chip can be programmed into memory.

In regards to Claim 25, Pfeiffer et al teaches in the abstract the use of an image processing apparatus. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Columns 9, Lines 7-22 that the image algorithm processor controls the requests for memory access of the image memory. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks. Pfeiffer et al teaches that the image algorithm processor controls the access requests from all of the image processors and teaches that the parallel processor set can perform more than one process. Therefore, enabling the image processing apparatus with control means to control another operation of the image processing apparatus. Pfeiffer et al teaches on Columns 20, Lines 27-46 that a portion of the image memory is not viewable and allows image processing data, such as coefficients, intermediate results or instructions to be stored in the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor Pfeiffer et al teaches

that no two address requests can request access to the image memory simultaneously. Therefore, the access request to store image processing instructions to the image memory will be carried out at a time other than a time during which a refresh process, first process, or second process access the image memory.

As for Claim 26, Pfeiffer et al teaches that the arbitrating means allows the DRAM refresh means to perform a DRAM refresh operation. The arbitrating means further disables the processes controlled by the image algorithm processor for the amount of time needed to complete the DRAM refresh command. Furthermore, if the control means needed to be operated, the operation would not start until the DRAM refresh command was complete. Furthermore, the control operation would be disabled when another DRAM refresh operation needed to be executed.

As for Claim 27, Pfeiffer et al teaches that the predetermined time period changes in that the time period for DRAM refresh during an operation for a screen refresh takes place during the horizontal planking periods and the time for DRAM refresh during a command from the image algorithm processor takes place at a periodic time and is given priority over the commands from the image algorithm processor.

In regards to Claim 28, Pfeiffer et al teaches on Column 22, Lines 33-54 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer teaches that the bus interface includes a number of registers, which can be programmed to control the refresh parameters of the video DRAMs.

In regards to Claim 29, Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches that the image algorithm processor controls the access requests from all of the image processors and teaches that the parallel processor set can perform more than one process. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

As for Claim 30, Claim 30 is rejected for reasons discussed related to Claim 1, since Claim 30 is substantively equivalent to Claim 1.

As for Claim 31, Pfeiffer et al teaches in the abstract the use of an image processing apparatus. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first

process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor. Therefore, the refresh cycle is synchronized with the horizontal synchronizing signal.

In regards to Claim 32, Claim 32 is rejected for reasons discussed related to Claim 31, since Claim 32 is substantively equivalent to Claim 31.

In regards to Claim 33, Claim 33 is rejected for reasons discussed related to Claim 18, since Claim 33 is substantively equivalent to Claim 18.

As for Claim 34, Claim 34 is rejected for reasons discussed related to Claim 33, since Claim 34 is substantively equivalent to Claim 33.

As for Claim 35, Claim 35 is rejected for reasons discussed related to Claim 36, since Claim 35 is substantively equivalent to Claim 36.

In regards to Claim 36, Claim 36 is rejected for reasons discussed related to Claim 20, since Claim 36 is substantively equivalent to Claim 20.

In regards to Claim 37, Pfeiffer et al teaches in the abstract the use of an image processing apparatus. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image

processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority, followed by refresh of the DRAM cells, and then address request from the image algorithm processor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

As for Claim 38, Claim 38 is rejected for reasons discussed related to Claim 37, since Claim 38 is substantively equivalent to Claim 37.

As for Claim 39, Claim 39 is rejected for reasons discussed related to Claim 18, since Claim 39 is substantively equivalent to Claim 18.

In regards to Claim 40, Claim 40 is rejected for reasons discussed related to Claim 39, since Claim 40 is substantively equivalent to Claim 39.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USPN 5,808,952 Fung et al; USPN 6,052,129 Fowler et al; USPN 6,205,524 Ng; USPN 6,330,645 Harriman; USPN 5,894,446 Ituo; USPN 5,253,214 Herrmann; USPN 5,805,300 Fukushima; USPN 5,448,310 Kopet et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M Hannett whose telephone number is 703-305-7880. The examiner can normally be reached on 9:00 am to 6:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-842-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is 703-308-6789.

James Hannett
Examiner
Art Unit 2612

JMH
November 18, 2002

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600